**IN THE CLAIMS:**

1. (Currently Amended) A clock board for a redundant clock distribution system, the clock board comprising:

a clock synthesizer configured to provide an input clock signal, wherein energy of the input clock signal is substantially concentrated around an input clock signal frequency; and

a spread spectrum unit coupled to receive the input clock signal from the clock synthesizer, wherein the spread spectrum unit is configured to frequency modulate the input clock signal, thereby producing an output clock signal, wherein energy of the output clock signal is spread over a range of frequencies, and wherein, when the clock board is operating as a master in a redundant clock distribution system having a master clock board and a slave clock board, the spread spectrum unit is enabled;

wherein the clock board is configured to disable the spread spectrum unit when operating as the slave clock board; and

wherein the clock board, when operating as the slave clock board, is configured to assume the role of the master responsive to a failure of the master clock board.

2. (Original) The clock board as recited in claim 1, wherein the range of frequencies is centered around the input clock signal frequency.

3. (Original) The clock board as recited in claim 1, wherein the range of frequencies extends from the input clock signal frequency down to a lower frequency.

4. (Original) The clock board as recited in claim 1, wherein the range of frequencies is a predetermined is based on a percentage of the input clock signal frequency.

5. (Original) The clock board as recited in claim 4, wherein the predetermined percentage is programmable.

6. (Cancelled).

7. (Original) The clock board as recited in claim 1, wherein the spread spectrum unit is coupled to provide the output clock signal to a buffer, and wherein the buffer is configured to provide the output clock signal to clocked circuits in a computer system.

8. (Original) The clock board as recited in claim 7, wherein the clock synthesizer is coupled to receive a feedback clock signal form the clock buffer.

9. (Original) The clock board as recited in claim 1, wherein the clock board includes a crystal configured to generate a crystal clock signal, and wherein the clock synthesizer is coupled to receive the crystal clock signal.

10. (Original) The clock board as recited in claim 1, wherein the clock synthesizer is configured to receive a reference clock signal from another clock board.

11. (Original) The clock board as recited in claim 1, wherein the clock buffer is configured to provide a reference clock signal to another clock board.

12. (Original) A computer system comprising:
a plurality of clocked circuits;
a first clock board coupled to the plurality of clocked circuits; and
a second clock board coupled to the plurality of clocked circuits;
wherein each of the first and second clock boards includes a clock synthesizer configured to provide an input clock signal, and a spread spectrum unit coupled to receive the input clock signal, wherein the spread spectrum unit is configured to frequency modulate the input clock signal, thereby producing an output clock signal, wherein energy of the output clock signal is spread over a range of frequencies;

wherein the first clock board is configured to operate as a master clock board and the second clock board is configured to act as a slave clock board, wherein energy of the input clock signal received by the master clock board is substantially concentrated around an input clock signal frequency, and wherein, responsive to a failure of the first clock board, the second clock board is configured to operate as the master clock board; and

wherein the spread spectrum unit of the master clock board is enabled and the spread spectrum unit of the slave clock board is disabled.

13. (Original) The computer system as recited in claim 12, wherein the range of frequencies is centered around the input clock signal frequency.

14. (Original) The computer system as recited in claim 12, wherein the range of frequencies extends from the input clock signal frequency down to a lower frequency.

15. (Original) The computer system as recited in claim 12, wherein the range of frequencies is based on a predetermined percentage of the input clock signal frequency.

16. (Original) The computer system as recited in claim 15, wherein the predetermined percentage is programmable.

17. (Original) The computer system as recited in claim 12, wherein each of the first and second clock boards includes a buffer, and wherein the spread spectrum unit of each of the first and second clock boards is coupled to provide its respective output clock signal to its respective buffer.

18. (Original) The computer system as recited in claim 17, wherein the buffer of each of the first and second clock boards is coupled to provide its respective output clock signal to clocked circuits in the computer system.

19. (Original) The computer system as recited in claim 17, wherein the clock synthesizer of each of the first and second clock boards is coupled to receive a feedback clock signal from its respective buffer.

20. (Original) The computer system as recited in claim 12, wherein each of the first and second clock boards includes a crystal configured to generate a crystal clock signal, and wherein the clock synthesizer of each of the first and second clock boards is coupled to receive the crystal clock signal from its respective crystal.

21. (Original) The computer system as recited in claim 12, wherein the clock synthesizer of the first clock board is coupled to receive a reference clock signal from the second clock board, and wherein the second clock board is coupled to receive a reference clock signal from the first clock board.